FORM PTO-1390 (REV. 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 367.40342X00 filed 07/13/01

U.S APPLICATION NO. (If known, see 37 CFR 1 5): 09/889232

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB00/00161	15 January 1999 (15.01.99)	15 January 1999 (15.01.99)

TITLE OF INVENTION: INTERFACE

APPLICANT(S) FOR DO/EO/US: HERIBERT LINDLAR; MARKUS SCHETELIG; PAUL BURGESS, OLAF JOERESSEN

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND or SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [ ] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [ ] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendment.
15. [ ] A substitute specification.
16. [X] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:

International Publication No. WO00/42744
PCT Request Form
International Search Report
International Prelilminary Examination Report
Figs. Table 1-2,1a-1c,2a-2c,3,4a-4b

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/889232	PCT/GB00/00161	367.40342X00

21. [X] The following fees are submitted:

	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a (2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	27 -20 =	7	x $18.00	$ 126.00	
Independent claims	5 -3 =	2	x $80.00	$ 160.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $270.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 1,146.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2. +				$ 0.00	
SUBTOTAL =				$ 1,146.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0.00	
TOTAL NATIONAL FEE =				$ 1,146.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0.00	
TOTAL FEES ENCLOSED =				$ 1,146.00	
				Amount to be refunded:	$
				charged:	$

a. [ ] A check in the amount of $ _____ to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 01-2135 . A duplicate copy of this sheet is enclosed.

d. [X] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

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NAME

26,422
REGISTRATION NUMBER

367.40342X00
PAT 99401US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Heribert LINDLAR et al

Serial No.: To Be Assigned

Filed: July 13 2001
(Concurrently Herewith)

For: INTERFACE

Art Unit: To Be Assigned

Examiner:

PRELIMINARY AMENDMENT

Assistant Commissioner
for Patents
Washington, D. C. 20231

July 13 2001

Sir:

Prior to examination of the above-identified application, please amend the claims as follows:

IN THE SPECIFICATION:

A Substitute Specification and a marked up version showing the changes made thereto is submitted herewith.

Also submitted herewith is a marked up version of the changes made to the claims.

IN THE CLAIMS:

Please amend the claims as follows

1. (Amended) A device having an interface for controlling RF transceiver circuitry, the interface comprising:

a plurality of connectors for controlling the RF transceiver circuitry including providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;

at least first and second further connectors wherein in a first mode, one of said first and second connectors supplies data to the transceiver and the other connector is operable to perform a first function and wherein, in the second mode, one of said first and second connectors receives data from said RF module and the other connector is operable to perform a second different function.

4. (Amended) A device as claimed in claim 1 wherein the first function is controlling the power amplifier of the transmitter portion of the transceiver.

5. (Amended) A device as claimed in claim 1 wherein said second function is the provision of a second control signal to the transceiver.

7. (Amended) A device as claimed in claim 1 wherein the second function is controlling dc estimation of the data received by the receiving portion of the transceiver.

8. (Amended) A device as claimed in claim 1 wherein said second function is the reception of data from the transceiver

9. (Amended) A device as claimed in claim 1 wherein the first connector is bi-directional and supplies data in the first mode and receives data in the second mode.

10. (Amended) A device as claimed in claim 1 wherein predetermined time critical control signals are not provided via said plurality of connectors.

11. (Amended) A device as claimed in claim 1 wherein the first mode is a transmit mode for the transceiver.

12. (Amended) A device as claimed in claim 1 wherein the second mode is a receive mode of the transceiver.

13. (Amended) A device as claimed in claim 1 wherein the plurality of connectors includes a connector for transferring data to and from the device, a connector for providing an enable signal from the device and a connector for providing a clock signal from the device.

14. (Amended) A device as claimed in claim 1 wherein the plurality of connectors are used to read from and write to registers in the transceiver

15. (Amended) A device as claimed in claim 1 wherein the plurality of connectors are a serial interface having at least one connector via which data is transmitted serially, said data including a device address, a bit indicating whether data is for writing or is to be read, a local address and a variable data portion.

16. (Amended) A device as claimed in claim 1, comprising first control circuitry and a processor, wherein the first control circuitry is arranged to control the RF circuitry via the plurality of connectors and/or the first and second further connectors and the processor is arranged to control the RF circuitry only via the plurality of connectors.

17. (Amended) A device as claimed in claim 15 wherein the data portion varies between 1 and 32 bits.

18. (Amended) A device as claimed in claim 1 wherein the plurality of connectors are coupled to at least one other device.

19. (Amended) A device as claimed in claim 1 comprising a connector for receiving a clock signal from the transceiver.

20. (Amended) A device as claimed in claim 1 comprising a third connector for powering down components of the transceiver.

21. (Amended) Transceiver circuitry having an interface for connection to a device having baseband circuitry, the interface comprising:
a plurality of connectors for providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;
at least first and second connectors wherein in a first mode, data is received at one of said first and second connectors and the other connector performs a first function and wherein, in the second mode, data is provided at one of said first and second connectors for transfer to the device and the other connector performs a second function different to the first.

22. (Amended) Transceiver circuitry as claimed in claim 21 comprising a power amplifier, wherein the first function is the reception of a first control signal for controlling the power amplifier.

23. (Amended) Transceiver circuitry as claimed in claim 21 comprising DC estimation circuitry wherein the second function is the reception of a second different control signal for controlling the dc estimation circuitry.

26. (Amended) A method of interfacing a device having a baseband circuitry to a transceiver, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the receiving mode;
receiving data at the device from the transceiver via the first connector; and
controlling the dc estimation in the transceiver via the second connector.

REMARKS

The claims have been amended to remove the multiple dependent claims before filing fee calculation.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (367.40342X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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DES:dlh

367.40342X00
PAT 99401US

VERSION WITH MARKINGS TO SHOW CHANGE MADE ACCOMPANYING PRELIMINARY AMENDMENT OF JULY 13, 2001

IN THE SPECIFICATION:

See the Marked Up Version of the Specification submitted herewith.

IN THE CLAIMS:

The claims were amended as follows:

1. (Amended) A device having an interface for controlling RF transceiver circuitry, the interface [having] comprising:
a plurality of connectors for controlling the RF transceiver circuitry including providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;
at least first and second further connectors wherein in a first mode, one of said first and second connectors supplies data to the transceiver and the other connector is operable to perform a first function and wherein, in the second mode, one of said first and second connectors receives data from said RF module and the other connector is operable to perform a second different function.

4. (Amended) A device as claimed in [any preceding] claim 1 wherein the first function is controlling the power amplifier of the transmitter portion of the transceiver.

5. (Amended) A device as claimed in [any preceding] claim 1 wherein said second function is the provision of a second control signal to the transceiver.

7. (Amended) A device as claimed in [any preceding] claim 1 wherein the second function is controlling dc estimation of the data received by the receiving portion of the transceiver.

8. (Amended) A device as claimed in [any one of claims 1 to 4] claim 1 wherein said second function is the reception of data from the transceiver

9. (Amended) A device as claimed in [any preceding] claim 1 wherein the first connector is bi-directional and supplies data in the first mode and receives data in the second mode.

10. (Amended) A device as claimed in [any preceding] claim 1 wherein predetermined time critical control signals are not provided via said plurality of connectors.

11. (Amended) A device as claimed in [any preceding] claim 1 wherein the first mode is a transmit mode for the transceiver.

12. (Amended) A device as claimed in [any preceding] claim 1 wherein the second mode is a receive mode of the transceiver.

13. (Amended) A device as claimed in [any preceding] claim 1 wherein the plurality of connectors includes a connector for transferring data to and from the device, a connector for providing[,] an enable signal from the device and a connector for providing a clock signal from the device.

14. (Amended) A device as claimed in [any preceding] claim 1 wherein the plurality of connectors are used to read from and write to registers in the transceiver

15. (Amended) A device as claimed in [any preceding] claim 1 wherein the plurality of connectors [is] are a serial interface having at least one connector via which data is transmitted serially, said data including a device address, a bit indicating whether data is for writing or is to be read, a local address and a variable data portion.

16. (Amended) A device as claimed in [any preceding] claim 1, further comprising first control circuitry and a processor, wherein the first control circuitry is arranged to control the RF circuitry via the plurality of connectors and/or the first and second further connectors and the processor is arranged to control the RF circuitry only via the plurality of connectors.

17. (Amended) A device as claimed in claim 15 wherein the data portion [may have a length varying] varies between 1 and 32 bits.

18. (Amended) A device as claimed in [any preceding] claim 1 wherein the plurality of connectors are coupled to at least one other device.

19. (Amended) A device as claimed in [any preceding] claim 1 [further] comprising a connector for receiving a clock signal from the transceiver.

20. (Amended) A device as claimed in [any preceding] claim 1 [having] comprising a third connector [(SleepX)] for powering down components of the transceiver.

21. (Amended) Transceiver circuitry having an interface for connection to a device having baseband circuitry, the interface [having] comprising:
a plurality of connectors for providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;
at least first and second connectors wherein in a first mode, data is received at one of said first and second connectors and the other connector performs a first

function and wherein, in the second mode, data is provided at one of said first and second connectors for transfer to the device and the other connector performs a second function different to the first.

22. (Amended) Transceiver circuitry as claimed in claim 21 [having] comprising a power amplifier, wherein the first function is the reception of a first control signal for controlling the power amplifier.

23. (Amended) Transceiver circuitry as claimed in claim 21 [or 22 having] comprising DC estimation circuitry wherein the second function is the reception of a second different control signal for controlling the dc estimation circuitry.

26. (Amended) A method of interfacing a device having a baseband [engine] circuitry to a transceiver, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the receiving mode;
receiving data at the device from the transceiver via the first connector; and
controlling the dc estimation in the transceiver via the second connector.

Interface

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an interface between base band circuitry and radio frequency transceiver circuitry, particularly circuitry operating in accordance with the Bluetooth Low Power Radio Frequency Specification. It additionally relates to devices having such an interface and either type of circuitry.

Description of the Prior Art

Low power radio frequency systems allow communication between devices over short distances typically ten's of meters. The devices must each be capable of receiving and transmitting according to the system's protocol.

One low power radio frequency system is the Bluetooth system. This system is designed to replace connecting wires and cables with wireless connectivity. For one device to communicate with another device, no wires connecting them will be necessary. Instead, each device will host a transceiver. A transceiver has a baseband part and an RF part. The host itself may have processing circuitry which is capable of doing the base band processing and that host will only require RF transceiver circuitry to be correctly connected to that processing circuitry.

SUMMARY OF THE INVENTION

It would be desirable to create RF transceiver circuitry that can be connected to many different hosts to provide the hosts with wireless connectivity.

It would be desirable to standardize the interface at which the connection between the base band circuitry and the transceiver circuitry is made making it vendor and platform independent.

It would be desirable to have a simple interface between the baseband part and the radio frequency part and in particular to have a reduced number of pins in the interface. A reduced number of pins provides the advantages of reduced chip area and reduced power consumption due to less toggling of pins.

Embodiments of the present invention therefore provide an interface with a low pin count and attendant low power consumption.

The low pin count arises out of: the burst mode controller and the microcontroller both using the DBus; the burst mode controller using the DBus for different tasks and the function of the RFBus being dependent upon the operational mode.

The burst mode controller controls time critical tasks in the RF circuitry using the DBus and RFBus. The DBus is used to control time critical configurations. The RFBus is used to transfer data and, in the transmit mode, to control the power amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention and to understand how the same may be brought into effect reference will now be made, by way of example only, to the accompanying tables and figures in which:

Table 1 illustrates the signals provided at the interface between Baseband (BB) circuitry and Radio Frequency (RF) circuitry;

Table 2 illustrates the effect of operational modes on the signals provided at the interface via RFBus;

Figure 1a illustrates the BB side of the RF-BB interface;

Figure 1b illustrates the RF side of the RF-BB interface;

Figure 1c is a schematic illustration of a LPRF transceiver illustrating the functionality of RFBus;

Figure 2a illustrates how the RFBus is configured and how the RF chip responds in the control mode;

Figure 2b illustrates how the RFBus is configured and how the RF chip responds in the transmit mode;

Figure 2c illustrates how the RFBus is configured and how the RF chip responds in the receive mode;

Figure 3 illustrates how the DBus may control devices in addition to an LPRF RF chip having RF circuitry;

Figure 4a illustrates Write Access on DBus;

Figure 4b illustrates Read Access on DBus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1a illustrates baseband (BB) circuitry 100 having an interface 10. The interface is connected or connectable to a similar corresponding interface 10 of radio frequency (RF) circuitry 200 illustrated in Figure 1b.

The interface 10 has seven pins. The pins 20, 22 and 24 are assigned to the bus of control signals DBus 12 and respectively transfer the signals DBusDa, DBusEnX and DBusClk. The pin 30 is assigned to the sleep control signal SleepX 14 . The pins 40, 42 and 44 are assigned to the bus of data signals RFBus 16 and respectively transfer the signals RFBus1, RFBus2 and BBClk.

The pins of the interface 10 in the BB circuitry connect or are connectable to corresponding pins of the interface 10 of the RF circuitry 200.

The DBus 12 has three signal lines associated with the pins 20, 22 and 24. A bi-directional signal line for transferring data signal DBusDa either from BB circuitry 100 to RF circuitry 200 or from RF circuitry 200 to BB circuitry 100, via pin 20. A unidirectional signal line is for transferring an enable signal DBusEnX from the BB circuitry 100 to RF circuitry 200, via pin 22. A unidirectional signal line is for transferring a clock signal DBusClk from the BB circuitry 100 to RF circuitry 200, via pin 24.

The RFBus 16 has three signal lines associated with the pins 40, 42 and 44. A bi-directional signal line is for transferring signal RFBus1 via pin 40. A unidirectional signal line is for transferring a clock signal BBCLK from the RF circuitry 200 to BB circuitry 100 via pin 44. A unidirectional signal line is for transferring signal RFBus2 from BB circuitry 100 to RF circuitry 200 via pin 42.

SleepX 14 is a unidirectional signal line for transferring from the BB circuitry 100 a signal SleepX for controlling power-down in the RF circuitry 200.

Table 1 illustrates the signals provided at the interface 10 and identifies each one of the interface signals by their associated interface pin, their name, their direction and their function.

DBus

DBus 12 is a serial I/O Data Bus. It is a Clock, Data, Enable serial interface. It is not dedicated purely to the interface 10 between the RF circuitry 200 and the BB circuitry 200. Figure 3, illustrates the situation in which the BB circuitry 100 is integrated into another host system. The BB circuitry 100 is the DBus Master. In this example the host system is a radio telephone 300, but it could

be a computer or personal digital assistant (PDA). The DBus 12 communicates with DBus Slaves. One DBus Slave is the RF circuitry 200 which is connected to DBus via the interface 10. Other slaves communicated with are in the example illustrated Power Supply Management Circuitry 310 and RF Modulator Circuitry 320 for the GSM protocol.

The DBus (DBusDa, DBusEnX and DBusClk) is used to control the RF circuitry and other devices as illustrated in Figure 4. The DBus writes control data to and reads control data from registers in the RF circuitry 200. The registers written to may include a register which controls the frequency at which the RF chip transmits or receives, a register which controls the power at which the RF chip transmits and registers which identify whether the RF chip is in the control, transmit or receive mode. The registers read from may include a register containing RSSI information. Thus the DBus may control the operation of the RF circuitry, for example, controlling the transition from receiving to transmitting.

The BB circuitry 100 controls access to the DBus. The BB circuitry precedes transferred data words with a device address, a Read/Write (R/W) identification bit and a register address. Each device address is 3 bits long allowing for 8 devices (the RF circuitry 200 and 7 others) to be accessed. The R/W bit when LOW indicates the BB circuitry is to write to the addressed register and when HIGH indicates that the BB circuitry is to read from the addressed register. The register address is 5 bits long allowing 32 registers to be addressed. The data words may be of variable length and may have a practical limit of 32 bits. Data words of 16 bits are preferred for transfer to/from the RF circuitry 200.

Address bits and R/W bit are verified before latching data to permit bus sharing with devices which are used concurrently to RF circuitry 200.

Access via DBus is enabled by taking DBusEnX at a LOW half of a clock cycle before the first positive clock edge of DBusClk. At the first rising edge of DBusClk the MSB of the device address will be clocked from DBusDa into the DBus Slave.

A write access is illustrated in Figure 4b. To write to RF circuitry 200, the DBus Master circuitry 100 places data onto DBusDa at the falling edge of DBusClk. The DBus Slave 200 having verified that it is addressed takes data from DBusDa on each of the rising edges of DBusClk. The DBus Master 100 changes the state of data at the falling edge of each clock pulse of DBusClk. Following the 8 address bits and R/W bit, data bits are sent with the same timing as the address bits. Following the last data bit the enable line DBusEnX is taken HIGH. The clock then pulses one more pulse and is then held LOW for a minimum of one cycle before a new access may be started. The enable DBusEnX is therefore held HIGH for a minimum of two cycles.

A read access is illustrated in Figure 4a. The DBus Slave when being read from, places data onto DBusDa on each of the rising edges of DBusClk. The data is read from DBusDa by the DBus Master 100 on each of the falling edge of DBusClk. During a read access the addressed device generates data on the DBus to be read by the controlling device. Following the 8 address bits and R/W bit there is a turn around bit which lasts for half a clock cycle and has the effect of realigning the DBus timing such that the addressed device will load bits onto the DBus upon the rising edge of the DBusClk. The bits are read at the DBus Master 100 on the falling edges of the DBusClk. Following the last data bit, the DBusClk is disabled for at least one clock cycle before the next access. The data word length is not fixed. The DBus Master 100 controls DBusEnX. The number of data bits and the data word length is fixed for a certain address by convention.

RFBus

The interface 10 has a dedicated pin for signal RFBus1, a dedicated pin for signal RFBus2; and a dedicated pin for clock signal BBClk (13MHz), used to synchronize data transferred via RFBus. BBClk may also be used for clocking logic of BB circuitry 100. BBClk is generated by RF circuitry 200 at 13MHz for symbol rate of 1Mbaud @ 13 fold oversampling.

The RFBus 16 is multifunctional. The RFBus is used for transferring received data from the RF circuitry 200 to the BB circuitry 100, transferring data for transmission from the BB circuitry 100 to the RF circuitry 200 and transferring control data between the BB circuitry 100 and RF circuitry 200. The ability of the RFBus to transfer control data is used for different purposes depending upon the operational mode of the system.

The RFBus 1 is bi-directional. In a Transmit mode the RFBus 1 provides data to the RF circuitry 200 for transmission. In a Receive Mode RFBus 2 receives data from the RF circuitry 200. Although in the examples given a single data signal RFBus1 is illustrated, a plurality of such data signals may be used to increase bandwidth.

The RFBus 2 is used to control time critical tasks in the RF circuitry 200. Time critical tasks are tasks which need to be effected on a time scale of less than 1 bit width (1 μs in Bluetooth). The RFBus2 is fast (13 MHz) at transmitting control signals from the BB circuitry 100 to the RF circuitry 200. In the Transmit mode, RFBus2 is used to control the timing of the Power Amplifier. In the Receive Mode the RFBus 2 is used to control the timing of the DC estimator changing from a fast data acquisition mode to a slower data acquisition mode.

The operational mode of the system is determined by the BB circuitry 100. The BB circuitry indicates a change of mode to the RF circuitry 200 via DBus. The modes include Transmit Mode, Receive Mode and Control Mode.

Interface of BB circuitry

The BB circuitry illustrated in Figure 1a has the interface 10 previously described. It additionally has a Serial Control Interface 110, a Burst Mode Controller (BMC) including a Timing Control Unit 130, a microcontroller 140, a sleep mode controller 150 and clock distribution circuitry (CDC) 160. The Serial Control Interface 110 provides DBus at pins 20, 22 and 24. The Burst Mode Controller 120 provides RFBus1 at pin 40 and RFBus2 at pin 42. The Sleep Mode Controller provides SleepX at pin 30. The Clock Distribution Circuitry (CDC) 160 is connected to pin 44 of interface 10 and receives BBClk from the RF circuitry 200.

The CDC 160 provides clock signals derived from BBClk to the BMC 120, the microcontroller 140 and the Serial Control Interface 110.

The Serial Control Interface 110 is controlled to produce DBus by either the microcontroller 140 or the Burst Mode Controller 120. The Burst Mode Controller controls DBus when time critical configurations to RF circuitry 200 are made. Whether the microcontroller 140 or the BMC 120 controls the content of DBus is determined by a switch signal 142 provided by the microcontroller 140 to the Serial Control Interface 110. The BMC 120 provides Data information 122, address information 124 and R/W information 126 to the Serial Control Interface 110 which places this information in the correct serial format on DBusDa. The clock signal DBusClk (13MHz) is received from CDC 160. The timing of the transitions in the Enable signal DBusEnX are controlled by a Trigger signal 132 provided by the Timing Control Unit 130 in the BMC 120.

The Burst Mode Controller 120 controls the content of RFBus1 and RFBus2 and may additionally control the content of DBus. The Burst Mode Controller directly provides RFBus2 to pin 42 and provides RFBus1 to pin 40 in the Transmit Mode and receives RFBus1 from pin 40 in the Receive Mode.

The microcontroller may access the DBus and hence the RF circuitry via the Serial Control Interface. When the DBus is controlled by the microcontroller no time critical tasks can be controlled via the DBus. This configuration is used in the boot phase or for RSSI measurement. When the BMC 120 controls the DBus, it is possible to control time critical tasks via the DBus. The ability of the BMC 120 to control time critical tasks via the DBus depends upon the resolution of the trigger signal 132 which is at least 1μs. The control signals sent by the BMC 120 via RFBus2 may have an even higher resolution if they are directly clocked by BBClk @ 13MHz.

Interface of RF circuitry

Fig 1b illustrates the RF circuitry 200 which has an interface 10. The interface has pins 20, 22 and 24 dedicated respectively to DBusDa, DBusEnX and DBusClk, pin 30 dedicated to SleepX and pins 40, 42 and 44 respectively dedicated to RFBus1, RFBus2 and BBClk. The RF circuitry 200 includes a Control Interface 210; a register set 220 illustratively including registers 222, 224 and 226; decoding circuitry 230; a NOT gate 232; a two input AND gate 234; a three input OR gate 236; power-supply regulator circuitry 240; a reference oscillator 250; switching circuitry 260; Transmission Path 270 and Reception Path 280.

The Control Interface 210 has an input interface 212 connected to DBus and a input 214 for receiving Sleep X. It has an output 216 for supplying a mode control signal to the input of decoding circuitry 230 and to the control input 262 of the switching circuitry 260 and an interface 218 for accessing the set of registers 220. The Control Interface 210 receives DBus and performs the

appropriate action which may involve writing to a register or reading from a register and changing the mode of operation of the RF circuitry 200. By writing to appropriate registers the Control Interface 210 may control the operational mode of the RF circuitry 200, control the synthesizer frequency in the Tx or Rx path, control whether the RF circuitry should receive or transmit, and control the power at which the Tx path 270 should transmit. By reading from appropriate registers, information concerning received signal quality such as RSSI can sent by the Control Interface 210 to the BB circuitry 100. For simplicity of illustration the operative connections of the Rx Path 280 and Tx Path 210 to the register set 220 are not shown. A two bit signal is provided at the output 216 indicating the operational mode- [10] indicates Receive Mode, [01] indicates Transmit Mode and [11] indicates Control Mode.

The switching circuitry 260 has an input 262 connected to output 216 of the Control Interface 210, a single primary interface and three secondary interfaces. The primary interface has one port connected to pin 40 to transfer RFBus1 and another port connected to pin 42 to transfer RFBus2. One of the secondary interfaces is connected at any one time to the primary interface in dependence on the signal received at the input 262. When the signal at input 262 indicates Control Mode, a port 264 of a first one of the secondary interfaces is connected to pin 40 via the switching circuitry 260. The port 264 is connected to one input of the AND gate 234. When the signal at input 262 indicates Transmit Mode, a port 266 of a different one of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 267 of that secondary interface is connected to pin 42 via the switching circuitry 260. When the signal at input 262 indicates Receive Mode a port 268 of another of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 269 of that secondary interface is connected to pin 42 via the switching circuitry 260. The ports 266 and 267 and 268 and 269 are connected to the Tx Path 270 and Rx Path 280 respectively as further illustrated in Figure 1c.

The decoding circuitry 230 has a 2 bit wide input connected to the output 216 of the Control Interface 210 and provides its output to one input of AND gate 234 and, via NOT gate 232, to one input of OR gate 236. The decoding circuitry 230 produces a HIGH output when the signal received at its input identifies the Control Mode and a LOW signal otherwise.

The OR gate receives one input via the NOT gate 232 as described, another input from the pin 30 which receives SleepX and a final input from the output of AND gate 234. The output of the OR gate 236 is provided as a standby control signal to the Power-Supply Regulation Circuitry 240 and to the Reference Oscillator 250. A LOW output from the OR gate 236 places Power-Supply Regulation Circuitry 240 into a low power consumption standby state and switches the Reference Oscillator 250 off.

The Reference Oscillator 250 provides its output to the pin 44. It's output is also used elsewhere within the RF circuitry, but this is not illustrated for purposes of clarity.

Figure 1c illustrates the control effected on the Tx path 270 during Transmit Mode and the control effected on the Rx Path 280 during Receive Mode.

The Transmit path 270 includes Pulse Shaping Circuitry 272 which receives an input from port 266 of switching circuitry 260 in the Transmit Mode and otherwise does not receive an input. The output of the Pulse Shaping Circuitry 272 is provided as an input to Modulation Circuitry 274 which provides the modulated signal to Power Amplifier 276 for amplification and subsequent transmission via an antenna. The power Amplifier 276 has a control input by which the amplifier gain may be forced to ramp up or ramp down. This control input is connected to port 267 of the switching circuitry 260. The power amplifier can therefore be switched on or off.

The Receive Path 280 includes Frequency Down Conversion Circuitry 286 which receives an input from the antenna in the Receive Mode. The circuitry 286 converts the received signal to a lower frequency and provides it to Demodulation Circuitry 284. The demodulated signal is provided to DC estimation circuitry 282. The amplitude decided data output by DC Estimation circuitry 282 is supplied to the port 268 of the switching circuitry 260. The DC Estimation Circuitry 282 has a control input connected to the port 269 of switching circuitry 260. The signals provided at the control input determine whether the DC Estimation operates in a fast mode or a slow mode.

Operational Modes

In the Transmit Mode, as illustrated in Figure 2b, RFBus1 and RFBus2 are driven by BB circuitry 100. RFBus1 supplies digital data for transmission <TXDATA> from BB circuitry 100 to RF circuitry 200 via pin 40. Logic levels are used and pulse shaping is done completely in RF circuitry 200. RFBus2 controls the timing of powering up the Power Amplifier (PA) in the RF circuitry 200 using control signal <PAON>. When RFBus2=<PAON>=HIGH the Power Amplifier is on when RFBus2=<PAON>=LOW the Power Amplifier is off. The switching on and off of the Power Amplifier is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 μs for Bluetooth Specification 1.0).

In Receive Mode, as illustrated in Figure 2c, RFBus1 is driven by RF circuitry 200 and RFBus2 driven by BB circuitry 100. RFBus1 supplies received data <RXDATA> to the BB circuitry 100 via pin 40. RFBus2 controls DC estimation in RF circuitry 200 via pin 42. The switching of DC estimation is 'time critical' as it occurs on a time scale of less than 1 slot duration. <DCTRACK>=LOW cause use of a fast acquisition of a DC estimate which is typically used at the start of a received packet and <DCTRACK>=HIGH controls use of a slower

DC estimation which is typically used for the remainder of the packet. The change of DC estimation is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 μs for Bluetooth Specification 1.0).

The Control Mode is the neutral mode entered when neither the Transmit Mode or Receive Mode are active. It is entered when SleepX is LOW or via a control word on DBus. In this mode, as illustrated in Figure 2a, RFBus1 and RFBus2 are driven by BB circuitry 100: RFBus2 does not have an assigned functionality; RFBus1= <ClkOn>. When RFBus1=<ClkOn>=HIGH, AND gate 234 switches ON the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240. When RFBus1=<ClkOn>=LOW, AND gate 234 switches OFF the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240 into standby. The RF circuitry is placed in a low power mode. There is no activity on DBus and RFBus and BBClk is switched off.

It will therefore be appreciated that the RFBus is used for different purposes during different operational modes of the system, as illustrated in Figures 2a, 2b, and 2c and Table 2.

The operation of a LPRF device is described in detail in UK Patent Application No 9820859.8 , the contents of which are hereby incorporated by reference. In particular Figure 4 shows LPRF RF components of a transceiver (Tx, Rx and Frequency control), connected to baseband components (the remaining elements in the Figure).

In the preceding described embodiment, the receive path 280 was partitioned so that the DC Estimation circuitry 282 was in the RF Circuitry 200. This results in RFBus1, during the receive mode, transferring RxData from the RF Circuitry 200 to the BB circuitry 100 across interface 10 and RFBus2 transferring a control signal, DcTrack, from the BB circuitry 100 to RF

Circuitry 200 across interface 10. This partitioning of the receive path is not essential.

In a second contemplated embodiment, the DC Estimation circuitry 282 is located within the baseband circuitry 100. This results in RFBus2 having a different directional flow than described above in the receive mode. In the second embodiment, the DCTrack signal is wholly within the baseband circuitry 100 and is not provided at the interface 10. The analog output of the demodulator 284 is converted to a digital signal for example by a sigma-delta converter whose outputs are mapped to RFBus1 and RFBus2. Consequently, in this embodiment, data flows on both RFBus1 and RFBus2 from the RF circuitry 200 to the baseband circuitry 100 via interface 10 during the receive mode.

It is further contemplated that RF circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

It is further contemplated that BB circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or implicitly or any generalization thereof.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made to the foregoing description without departing from the scope of the invention.

Interface

BACKGROUND OF THE INVENTION
Field of the Invention

The present invention relates to an interface between base band circuitry and radio frequency transceiver circuitry, particularly circuitry operating in accordance with the Bluetooth Low Power Radio Frequency Specification. It additionally relates to devices having such an interface and either type of circuitry.

Description of the Prior Art

Low power radio frequency systems allow communication between devices over short distances typically ten's of meters. The devices must each be capable of receiving and transmitting according to the system's protocol.

One low power radio frequency system is the Bluetooth system. This system is designed to replace connecting wires and cables with wireless connectivity. For one device to communicate with another device, no wires connecting them will be necessary. Instead, each device will host a transceiver. A transceiver has a baseband part and an RF part. The host itself may have processing circuitry which is capable of doing the base band processing and that host will only require RF transceiver circuitry to be correctly connected to that processing circuitry.

SUMMARY OF THE INVENTION

It would be desirable to create RF transceiver circuitry that can be connected to many different hosts to provide the hosts with wireless connectivity.

It would be desirable to standardize the interface at which the connection between the base band circuitry and the transceiver circuitry is made making it vendor and platform independent.

It would be desirable to have a simple interface between the baseband part and the radio frequency part and in particular to have a reduced number of pins in the interface. A reduced number of pins provides the advantages of reduced chip area and reduced power consumption due to less toggling of pins.

According to one aspect of the present invention there is provided a device as claimed in claim 1.

According to another aspect of the invention there is provided transceiver circuitry as claimed in claim 21.

According to further aspects of the invention there is provided a method according to any one of claims 25 and 26.

According to a still further aspect of the invention there is provided an interface as claimed in claim 27.

Embodiments of the present invention therefore provide an interface with a low pin count and attendant low power consumption.

The low pin count arises out of: the burst mode controller and the microcontroller both using the DBus; the burst mode controller using the DBus for different tasks and the function of the RFBus being dependent upon the operational mode.

The burst mode controller controls time critical tasks in the RF circuitry using the DBus and RFBus. The DBus is used to control time critical configurations. The RFBus is used to transfer data and, in the transmit mode, to control the power amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention and to understand how the same may be brought into effect reference will now be made, by way of example only, to the accompanying tables and figures in which:

Table 1 illustrates the signals provided at the interface between Baseband (BB) circuitry and Radio Frequency (RF) circuitry;

Table 2 illustrates the effect of operational modes on the signals provided at the interface via RFBus;

Figure 1a illustrates the BB side of the RF-BB interface;

Figure 1b illustrates the RF side of the RF-BB interface;

Figure 1c is a schematic illustration of a LPRF transceiver illustrating the functionality of RFBus;

Figure 2a illustrates how RFBus is configured and how the RF chip responds in the control mode;

Figure 2b illustrates how RFBus is configured and how the RF chip responds in the transmit mode;

Figure 2c illustrates how RFBus is configured and how the RF chip responds in the receive mode;

Figure 3 illustrates how the DBus may control devices in addition to an LPRF RF chip having RF circuitry;

Figure 4a illustrates Write Access on DBus;

Figure 4b illustrates Read Access on DBus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1a illustrates baseband (BB) circuitry 100 having an interface 10. The interface is connected or connectable to a similar corresponding interface 10 of radio frequency (RF) circuitry 200 illustrated in Figure 1b.

The interface 10 has seven pins. The pins 20, 22 and 24 are assigned to the bus of control signals DBus 12 and respectively transfer the signals DBusDa, DBusEnX and DBusClk. The pin 30 is assigned to the sleep control signal

SleepX 14 . The pins 40, 42 and 44 are assigned to the bus of data signals RFBus 16 and respectively transfer the signals RFBus1, RFBus2 and BBClk. The pins of the interface 10 in the BB circuitry connect or are connectable to corresponding pins of the interface 10 of the RF circuitry 200.

The DBus 12 has three signal lines associated with the pins 20, 22 and 24. A bi-directional signal line for transferring data signal DBusDa either from BB circuitry 100 to RF circuitry 200 or from RF circuitry 200 to BB circuitry 100, via pin 20. A unidirectional signal line for transferring an enable signal DBusEnX from the BB circuitry 100 to RF circuitry 200, via pin 22. A unidirectional signal line for transferring a clock signal DBusClk from the BB circuitry 100 to RF circuitry 200, via pin 24.

The RFBus 16 has three signal lines associated with the pins 40, 42 and 44. A bi-directional signal line for transferring signal RFBus1 via pin 40. A unidirectional signal line for transferring a clock signal BBCLK from the RF circuitry 200 to BB circuitry 100 via pin 44. A unidirectional signal line for transferring signal RFBus2 from BB circuitry 100 to RF circuitry 200 via pin 42.

SleepX 14 is a unidirectional signal line for transferring from the BB circuitry 100 a signal SleepX for controlling power-down in the RF circuitry 200.

Table 1 illustrates the signals provided at the interface 10 and identifies each one of the interface signals by their associated interface pin, their name, their direction and their function.

DBus

DBus 12 is a serial I/O Data Bus. It is a Clock, Data, Enable serial interface. It is not dedicated purely to the interface 10 between the RF circuitry 200 and the BB circuitry 200. Figure 3, illustrates the situation in which the BB circuitry

100 is integrated into another host system. The BB circuitry 100 is the DBus Master. In this example the host system is a radio telephone 300, but it could be a computer or personal digital assistant (PDA). The DBus 12 communicates with DBus Slaves. One DBus Slave is the RF circuitry 200 which is connected to DBus via the interface 10. Other slaves communicated with are in the example illustrated Power Supply Management Circuitry 310 and RF Modulator Circuitry 320 for the GSM protocol.

The DBus (DBusDa, DBusEnX and DBusClk) is used to control the RF circuitry and other devices as illustrated in Figure 4. The DBus writes control data to and reads control data from registers in the RF circuitry 200. The registers written to may include a register which controls the frequency at which the RF chip transmits or receives, a register which controls the power at which the RF chip transmits and registers which identify whether the RF chip is in the control, transmit or receive mode. The registers read from may include a register containing RSSI information. Thus the DBus may control the operation of the RF circuitry, for example, controlling the transition from receiving to transmitting.

The BB circuitry 100 controls access to the DBus. The BB circuitry precedes transferred data words with a device address, a Read/Write (R/W) identification bit and a register address. Each device address is 3 bits long allowing for 8 devices (the RF circuitry 200 and 7 others) to be accessed. The R/W bit when LOW indicates the BB circuitry is to write to the addressed register and when HIGH indicates that the BB circuitry is to read from the addressed register. The register address is 5 bits long allowing 32 registers to be addressed. The data words may be of variable length and may have a practical limit of 32 bits. Data words of 16 bits are preferred for transfer to/from the RF circuitry 200.

Address bits and R/W bit are verified before latching data to permit bus sharing with devices which are used concurrently to RF circuitry 200.

Access via DBus is enabled by taking DBusEnX LOW half a clock cycle before the first positive clock edge of DBusClk. At the first rising edge of DBusClk, the MSB of the device address will be clocked from DBusDa into the DBus Slave.

A write access is illustrated in Figure 4b. To write to RF circuitry 200, the DBus Master circuitry 100 places data onto DBusDa at the falling edge of DBusClk. The DBus Slave 200 having verified that it is addressed takes data from DBusDa on each of the rising edges of DBusClk. The DBus Master 100 changes the state of data at the falling edge of each clock pulse of DBusClk. Following the 8 address bits and R/W bit, data bits are sent with the same timing as the address bits. Following the last data bit the enable line DBusEnX is taken HIGH. The clock then pulses one more pulse and is then held LOW for a minimum of one cycle before a new access may be started. The enable DBusEnX is therefore held HIGH for a minimum of two cycles.

A read access is illustrated in Figure 4a. The DBus Slave when being read from, places data onto DBusDa on each of the rising edges of DBusClk. The data is read from DBusDa by the DBus Master 100 on each of the falling edge of DBusClk. During a read access the addressed device generates data on the DBus to be read by the controlling device. Following the 8 address bits and R/W bit there is a turn around bit which lasts for half a clock cycle and has the effect of realigning the DBus timing such that the addressed device will load bits onto the DBus upon the rising edge of the DBusClk. The bits are read at the DBus Master 100 on the falling edges of the DBusClk. Following the last data bit, the DBusClk is disabled for at least one clock cycle before the next access. The data word length is not fixed. The DBus Master 100 controls

DBusEnX. The number of data bits and the data word length is fixed for a certain address by convention.

RFBus

The interface 10 has a dedicated pin for signal RFBus1, a dedicated pin for signal RFBus2; and a dedicated pin for clock signal BBClk (13MHz), used to synchronize data transferred via RFBus. BBClk may also be used for clocking logic of BB circuitry 100. BBClk is generated by RF circuitry 200 at 13MHz for symbol rate of 1Mbaud @ 13 fold oversampling.

The RFBus 16 is multifunctional. RFBus is used for transferring received data from the RF circuitry 200 to the BB circuitry 100, transferring data for transmission from the BB circuitry 100 to the RF circuitry 200 and transferring control data between the BB circuitry 100 and RF circuitry 200. The ability of the RFBus to transfer control data is used for different purposes depending upon the operational mode of the system.

RFBus 1 is bi-directional. In a Transmit mode the RFBus 1 provides data to the RF circuitry 200 for transmission. In a Receive Mode RFBus 2 receives data from the RF circuitry 200. Although in the examples given a single data signal RFBus1 is illustrated, a plurality of such data signals may be used to increase bandwidth.

RFBus 2 is used to control time critical tasks in the RF circuitry 200. Time critical tasks are tasks which need to be effected on a time scale of less than 1 bit width (1 μs in Bluetooth). RFBus2 is fast (13 MHz) at transmitting control signals from the BB circuitry 100 to the RF circuitry 200. In the Transmit mode, RFBus2 is used to control the timing of the Power Amplifier. In the Receive Mode RFBus 2 is used to control the timing of the DC estimator changing from a fast data acquisition mode to a slower data acquisition mode.

The operational mode of the system is determined by the BB circuitry 100. The BB circuitry indicates a change of mode to the RF circuitry 200 via DBus. The modes include Transmit Mode, Receive Mode and Control Mode.

Interface of BB circuitry

The BB circuitry illustrated in Figure 1a has the interface 10 previously described, it additionally has a Serial Control Interface 110, a Burst Mode Controller (BMC) including a Timing Control Unit 130, a microcontroller 140, a sleep mode controller 150 and clock distribution circuitry (CDC) 160. The Serial Control Interface 110 provides DBus at pins 20, 22 and 24. The Burst Mode Controller 120 provides RFBus1 at pin 40 and RFBus2 at pin 42. The Sleep Mode Controller provides SleepX at pin 30. The Clock Distribution Circuitry 160 is connected to pin 44 of interface 10 and receives BBClk from the RF circuitry 200.

The CDC 160 provides clock signals derived from BBClk to the BMC 120, the microcontroller 140 and the Serial Control Interface 110.

The Serial Control Interface 110 is controlled to produce DBus by either the microcontroller 140 or the Burst Mode Controller 120. The Burst Mode Controller controls DBus when time critical configurations to RF circuitry 200 are made. Whether the microcontroller 140 or the BMC 120 controls the content of DBus is determined by a switch signal 142 provided by the microcontroller 140 to the Serial Control Interface 110. The BMC 120 provides Data information 122, address information 124 and R/W information 126 to the Serial Control Interface 110 which places this information in the correct serial format on DBusDa. The clock signal DBusClk (13MHz) is received from ~~Clock Distribution Circuitry~~. The timing of the transitions in the

Enable signal DBusEnX are controlled by a Trigger signal 132 provided by the Timing Control Unit 130 in the BMC 120.

The Burst Mode Controller 120 controls the content of RFBus1 and RFBus2 and may additionally control the content of DBus. It directly provides RFBus2 to pin 42 and provides RFBus1 to pin 40 in the Transmit Mode and receives RFBus1 from pin 40 in the Receive Mode.

The microcontroller may access the DBus and hence the RF circuitry via the Serial Control Interface. When the DBus is controlled by the microcontroller no time critical tasks can be controlled via the DBus. This configuration is used in the boot phase or for RSSI measurement. When the BMC 120 controls the DBus, it is possible to control time critical tasks via the DBus. The ability of the BMC 120 to control time critical tasks via the DBus depends upon the resolution of the trigger signal 132 which is at least 1μs. The control signals sent by the BMC 120 via RFBus2 may have an even higher resolution if they are directly clocked by BBClk @ 13MHz.

Interface of RF circuitry

Fig 1b illustrates the RF circuitry 200 which has an interface 10. The interface has pins 20, 22 and 24 dedicated respectively to DBusDa, DBusEnX and DBusClk, pin 30 dedicated to SleepX and pins 40, 42 and 44 respectively dedicated to RFBus1, RFBus2 and BBClk. The RF circuitry 200 includes a Control Interface 210; a register set 220 illustratively including registers 222, 224 and 226; decoding circuitry 230; a NOT gate 232; a two input AND gate 234; a three input OR gate 236; power-supply regulator circuitry 240; a reference oscillator 250; switching circuitry 260; Transmission Path 270 and Reception Path 280.

The Control Interface 210 has an input interface 212 connected to DBus and a input 214 for receiving Sleep X. It has an output 216 for supplying a mode control signal to the input of decoding circuitry 230 and to the control input 262 of the switching circuitry 260 and an interface 218 for accessing the set of registers 220. The Control Interface 210 receives DBus and performs the appropriate action which may involve writing to a register or reading from a register and changing the mode of operation of the RF circuitry 200. By writing to appropriate registers the Control Interface 210 may control the operational mode of the RF circuitry 200, control the synthesizer frequency in the Tx or Rx path, control whether the RF circuitry should receive or transmit, and control the power at which the Tx path 270 should transmit. By reading from appropriate registers, information concerning received signal quality such as RSSI can sent by the Control Interface 210 to the BB circuitry 100. For simplicity of illustration the operative connections of the Rx Path 280 and Tx Path 210 to the register set 220 are not shown. A two bit signal is provided at the output 216 indicating the operational mode- [10] indicates Receive Mode, [01] indicates Transmit Mode and [11] indicates Control Mode.

The switching circuitry 260 has an input 262 connected to output 216 of the Control Interface 210, a single primary interface and three secondary interfaces. The primary interface has one port connected to pin 40 to transfer RFBus1 and another port connected to pin 42 to transfer RFBus2. One of the secondary interfaces is connected at any one time to the primary interface in dependence on the signal received at the input 262. When the signal at input 262 indicates Control Mode, a port 264 of a first one of the secondary interfaces is connected to pin 40 via the switching circuitry 260. The port 264 is connected to one input of the AND gate 234. When the signal at input 262 indicates Transmit Mode, a port 266 of a different one of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 267 of that secondary interface is connected to pin 42 via the switching

circuitry 260. When the signal at input 262 indicates Receive Mode, a port 268 of another of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 269 of that secondary interface is connected to pin 42 via the switching circuitry 260. The ports 266 and 267 and 268 and 269 are connected to the Tx Path 270 and Rx Path 280 respectively as further illustrated in Figure 1c.

The decoding circuitry 230 has a 2 bit wide input connected to the output 216 of the Control Interface 210 and provides its output to one input of AND gate 234 and, via NOT gate 232, to one input of OR gate 236. The decoding circuitry 230 produces a HIGH output when the signal received at its input identifies the Control Mode and a LOW signal otherwise.

The OR gate receives one input via the NOT gate 232 as described, another input from the pin 30 which receives SleepX and a final input from the output of AND gate 234. The output of the OR gate 236 is provided as a standby control signal to the Power-Supply Regulation Circuitry 240 and to the Reference Oscillator 250. A LOW output from the OR gate 236 places Power-Supply Regulation Circuitry 240 into a low power consumption standby state and switches the Reference Oscillator 250 off.

The Reference Oscillator 250 provides its output to the pin 44. It's output is also used elsewhere within the RF circuitry, but this is not illustrated for purposes of clarity.

Figure 1c illustrates the control effected on the Tx path 270 during Transmit Mode and the control effected on the Rx Path 280 during Receive Mode.

The Transmit path 270 includes Pulse Shaping Circuitry 272 which receives an input from port 266 of switching circuitry 260 in the Transmit Mode and

otherwise does not receive an input. The output of the Pulse Shaping Circuitry 272 is provided as an input to Modulation Circuitry 274 which provides the modulated signal to Power Amplifier 276 for amplification and subsequent transmission via an antenna. The power Amplifier 276 has a control input by which the amplifier gain may be forced to ramp up or ramp down. This control input is connected to port 267 of the switching circuitry 260. The power amplifier can therefore be switched on or off.

The Receive Path 280 includes Frequency Down Conversion Circuitry 286 which receives an input from the antenna in the Receive Mode. The circuitry 286 converts the received signal to a lower frequency and provides it to Demodulation Circuitry 284. The demodulated signal is provided to DC estimation circuitry 282. The amplitude decided data output by DC Estimation circuitry 282 is supplied to the port 268 of the switching circuitry 260. The DC Estimation Circuitry 282 has a control input connected to the port 269 of switching circuitry 260. The signals provided at the control input determine whether the DC Estimation operates in a fast mode or a slow mode.

Operational Modes

In the Transmit Mode, as illustrated in Figure 2b, RFBus1 and RFBus2 are driven by BB circuitry 100. RFBus1 supplies digital data for transmission <TXDATA> from BB circuitry 100 to RF circuitry 200 via pin 40. Logic levels are used and pulse shaping is done completely in RF circuitry 200. RFBus2 controls the timing of powering up the Power Amplifier (PA) in the RF circuitry 200 using control signal <PAON>. When RFBus2=<PAON>=HIGH the Power Amplifier is on when RFBus2=<PAON>=LOW the Power Amplifier is off. The switching on and off of the Power Amplifier is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 μs for Bluetooth Specification 1.0).

In Receive Mode, as illustrated in Figure 2c, RFBus1 is driven by RF circuitry 200 and RFBus2 driven by BB circuitry 100. RFBus1 supplies received data <RXDATA> to the BB circuitry 100 via pin 40. RFBus2 controls DC estimation in RF circuitry 200 via pin 42. The switching of DC estimation is 'time critical' as it occurs on a time scale of less than 1 slot duration. <DCTRACK>=LOW cause use of a fast acquisition of a DC estimate which is typically used at the start of a received packet and <DCTRACK>=HIGH controls use of a slower DC estimation which is typically used for the remainder of the packet. The change of DC estimation is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 µs for Bluetooth Specification 1.0).

The Control Mode is the neutral mode entered when neither the Transmit Mode or Receive Mode are active. It is entered when SleepX is LOW or via a control word on DBus. In this mode, as illustrated in Figure 2a, RFBus1 and RFBus2 are driven by BB circuitry 100: RFBus2 does not have an assigned functionality; RFBus1= <ClkOn>. When RFBus1=<ClkOn>=HIGH, AND gate 234 switches ON the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240. When RFBus1=<ClkOn>=LOW, AND gate 234 switches OFF the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240 into standby. The RF circuitry is placed in a low power mode. There is no activity on DBus and RFBus and BBClk is switched off.

It will therefore be appreciated that the RFBus is used for different purposes during different operational modes of the system, as illustrated in Figures 2a, 2b, and 2c and Table 2.

The operation of a LPRF device is described in detail in UK Patent Application No 9820859.8 , the contents of which are hereby incorporated by reference. In particular Figure 4 shows LPRF RF components of a transceiver (Tx, Rx

and Frequency control), connected to baseband components (the remaining elements in the Figure).

In the preceding described embodiment, the receive path 280 was partitioned so that the DC Estimation circuitry 282 was in the RF Circuitry 200. This results in RFBus1, during the receive mode, transferring RxData from the RF Circuitry 200 to the BB circuitry 100 across interface 10 and RFBus2 transferring a control signal, DcTrack, from the BB circuitry 100 to RF Circuitry 200 across interface 10. This partitioning of the receive path is not essential.

In a second contemplated embodiment, the DC Estimation circuitry 282 is located within the baseband circuitry 100. This results in RFBus2 having a different directional flow than described above in the receive mode. In the second embodiment, the DCTrack signal is wholly within the baseband circuitry 100 and is not provided at the interface 10. The analog output of the demodulator 284 is converted to a digital signal for example by a sigma-delta converter whose outputs are mapped to RFBus1 and RFBus2. Consequently, in this embodiment, data flows on both RFBus1 and RFBus2 from the RF circuitry 200 to the baseband circuitry 100 via interface 10 during the receive mode.

It is further contemplated that RF circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

It is further contemplated that BB circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

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The present invention relates to an interface between base band circuitry and radio frequency transceiver circuitry, particularly circuitry operating in accordance with the Bluetooth Low Power Radio Frequency Specification. It additionally relates to devices having such an interface and either type of circuitry.

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It would be desirable to create RF transceiver circuitry that can be connected to many different hosts to provide the hosts with wireless connectivity.

It would be desirable to standardize the interface at which the connection between the base band circuitry and the transceiver circuitry is made making it vendor and platform independent.

It would be desirable to have a simple interface between the baseband part and the radio frequency part and in particular to have a reduced number of pins in the interface. A reduced number of pins provides the advantages of reduced chip area and reduced power consumption due to less toggling of pins.

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According to a still further aspect of the invention there is provided an interface as claimed in claim 27.

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The low pin count arises out of: the burst mode controller and the microcontroller both using the DBus; the burst mode controller using the DBus for different tasks and the function of the RFBus being dependent upon the operational mode.

The burst mode controller controls time critical tasks in the RF circuitry using the DBus and RFBus. The DBus is used to control time critical configurations. The RFBus is used to transfer data and, in the transmit mode, to control the power amplifier.

For a better understanding of the present invention and to understand how the same may be brought into effect reference will now be made, by way of example only, to the accompanying tables and figures in which:

Table 1 illustrates the signals provided at the interface between Baseband (BB) circuitry and Radio Frequency (RF) circuitry;

Table 2 illustrates the effect of operational modes on the signals provided at the interface via RFBus;

Figure 1a illustrates the BB side of the RF-BB interface;

Figure 1b illustrates the RF side of the RF-BB interface;

Figure 1c is a schematic illustration of a LPRF transceiver illustrating the functionality of RFBus;

Figure 2a illustrates how RFBus is configured and how the RF chip responds in the control mode;

Figure 2b illustrates how RFBus is configured and how the RF chip responds in the transmit mode;

Figure 2c illustrates how RFBus is configured and how the RF chip responds in the receive mode;

Figure 3 illustrates how the DBus may control devices in addition to an LPRF RF chip having RF circuitry;

Figure 4a illustrates Write Access on DBus;

Figure 4b illustrates Read Access on DBus.

Figure 1a illustrates baseband (BB) circuitry 100 having an interface 10. The interface is connected or connectable to a similar corresponding interface 10 of radio frequency (RF) circuitry 200 illustrated in Figure 1b.

The interface 10 has seven pins. The pins 20, 22 and 24 are assigned to the bus of control signals DBus 12 and respectively transfer the signals DBusDa, DBusEnX and DBusClk. The pin 30 is assigned to the sleep control signal

SleepX 14 . The pins 40, 42 and 44 are assigned to the bus of data signals RFBus 16 and respectively transfer the signals RFBus1, RFBus2 and BBClk. The pins of the interface 10 in the BB circuitry connect or are connectable to corresponding pins of the interface 10 of the RF circuitry 200.

The DBus 12 has three signal lines associated with the pins 20, 22 and 24. A bi-directional signal line for transferring data signal DBusDa either from BB circuitry 100 to RF circuitry 200 or from RF circuitry 200 to BB circuitry 100, via pin 20. A unidirectional signal line for transferring an enable signal DBusEnX from the BB circuitry 100 to RF circuitry 200, via pin 22. A unidirectional signal line for transferring a clock signal DBusClk from the BB circuitry 100 to RF circuitry 200, via pin 24.

The RFBus 16 has three signal lines associated with the pins 40, 42 and 44. A bi-directional signal line for transferring signal RFBus1 via pin 40. A unidirectional signal line for transferring a clock signal BBCLK from the RF circuitry 200 to BB circuitry 100 via pin 44. A unidirectional signal line for transferring signal RFBus2 from BB circuitry 100 to RF circuitry 200 via pin 42.

SleepX 14 is a unidirectional signal line for transferring from the BB circuitry 100 a signal SleepX for controlling power-down in the RF circuitry 200.

Table 1 illustrates the signals provided at the interface 10 and identifies each one of the interface signals by their associated interface pin, their name, their direction and their function.

DBus

DBus 12 is a serial I/O Data Bus. It is a Clock, Data, Enable serial interface. It is not dedicated purely to the interface 10 between the RF circuitry 200 and the BB circuitry 200. Figure 3, illustrates the situation in which the BB circuitry

100 is integrated into another host system. The BB circuitry 100 is the DBus Master. In this example the host system is a radio telephone 300, but it could be a computer or personal digital assistant (PDA). The DBus 12 communicates with DBus Slaves. One DBus Slave is the RF circuitry 200 which is connected to DBus via the interface 10. Other slaves communicated with are in the example illustrated Power Supply Management Circuitry 310 and RF Modulator Circuitry 320 for the GSM protocol.

The DBus (DBusDa, DBusEnX and DBusClk) is used to control the RF circuitry and other devices as illustrated in Figure 4. The DBus writes control data to and reads control data from registers in the RF circuitry 200. The registers written to may include a register which controls the frequency at which the RF chip transmits or receives, a register which controls the power at which the RF chip transmits and registers which identify whether the RF chip is in the control, transmit or receive mode. The registers read from may include a register containing RSSI information. Thus the DBus may control the operation of the RF circuitry, for example, controlling the transition from receiving to transmitting.

The BB circuitry 100 controls access to the DBus. The BB circuitry precedes transferred data words with a device address, a Read/Write (R/W) identification bit and a register address. Each device address is 3 bits long allowing for 8 devices (the RF circuitry 200 and 7 others) to be accessed. The R/W bit when LOW indicates the BB circuitry is to write to the addressed register and when HIGH indicates that the BB circuitry is to read from the addressed register. The register address is 5 bits long allowing 32 registers to be addressed. The data words may be of variable length and may have a practical limit of 32 bits. Data words of 16 bits are preferred for transfer to/from the RF circuitry 200.

Address bits and R/W bit are verified before latching data to permit bus sharing with devices which are used concurrently to RF circuitry 200.

Access via DBus is enabled by taking DBusEnX LOW half a clock cycle before the first positive clock edge of DBusClk. At the first rising edge of DBusClk the MSB of the device address will be clocked from DBusDa into the DBus Slave.

A write access is illustrated in Figure 4b. To write to RF circuitry 200 the DBus Master circuitry 100 places data onto DBusDa at the falling edge of DBusClk. The DBus Slave 200 having verified that it is addressed takes data from DBusDa on each of the rising edges of DBusClk. The DBus Master 100 changes the state of data at the falling edge of each clock pulse of DBusClk. Following the 8 address bits and R/W bit, data bits are sent with the same timing as the address bits. Following the last data bit the enable line DBusEnX is taken HIGH. The clock then pulses one more pulse and is then held LOW for a minimum of one cycle before a new access may be started. The enable DBusEnX is therefore held HIGH for a minimum of two cycles.

A read access is illustrated in Figure 4a. The DBus Slave when being read from, places data onto DBusDa on each of the rising edges of DBusClk. The data is read from DBusDa by the DBus Master 100 on each of the falling edge of DBusClk. During a read access the addressed device generates data on the DBus to be read by the controlling device. Following the 8 address bits and R/W bit there is a turn around bit which lasts for half a clock cycle and has the effect of realigning the DBus timing such that the addressed device will load bits onto the DBus upon the rising edge of the DBusClk. The bits are read at the DBus Master 100 on the falling edges of the DBusClk. Following the last data bit the DBusClk is disabled for at least one clock cycle before the next access. The data word length is not fixed. The DBus Master 100 controls

DBusEnX. The number of data bits and the data word length is fixed for a certain address by convention.

RFBus

The interface 10 has a dedicated pin for signal RFBus1, a dedicated pin for signal RFBus2; and a dedicated pin for clock signal BBClk (13MHz), used to synchronize data transferred via RFBus. BBClk may also be used for clocking logic of BB circuitry 100. BBClk is generated by RF circuitry 200 at 13MHz for symbol rate of 1Mbaud @ 13 fold oversampling.

The RFBus 16 is multifunctional. RFBus is used for transferring received data from the RF circuitry 200 to the BB circuitry 100, transferring data for transmission from the BB circuitry 100 to the RF circuitry 200 and transferring control data between the BB circuitry 100 and RF circuitry 200. The ability of the RFBus to transfer control data is used for different purposes depending upon the operational mode of the system.

RFBus 1 is bi-directional. In a Transmit mode the RFBus 1 provides data to the RF circuitry 200 for transmission. In a Receive Mode RFBus 2 receives data from the RF circuitry 200. Although in the examples given a single data signal RFBus1 is illustrated a plurality of such data signals may be used to increase bandwidth.

RFBus 2 is used to control time critical tasks in the RF circuitry 200. Time critical tasks are tasks which need to be effected on a time scale of less than 1 bit width (1 μs in Bluetooth). RFBus2 is fast (13 MHz) at transmitting control signals from the BB circuitry 100 to the RF circuitry 200. In the Transmit mode, RFBus2 is used to control the timing of the Power Amplifier. In the Receive Mode RFBus 2 is used to control the timing of the DC estimator changing from a fast data acquisition mode to a slower data acquisition mode.

The operational mode of the system is determined by the BB circuitry 100. The BB circuitry indicates a change of mode to the RF circuitry 200 via DBus. The modes include Transmit Mode, Receive Mode and Control Mode.

Interface of BB circuitry

The BB circuitry illustrated in Figure 1a has the interface 10 previously described, it additionally has a Serial Control Interface 110, a Burst Mode Controller (BMC) including a Timing Control Unit 130, a microcontroller 140, a sleep mode controller 150 and clock distribution circuitry (CDC) 160. The Serial Control Interface 110 provides DBus at pins 20, 22 and 24. The Burst Mode Controller 120 provides RFBus1 at pin 40 and RFBus2 at pin 42. The Sleep Mode Controller provides SleepX at pin 30. The Clock Distribution Circuitry 160 is connected to pin 44 of interface 10 and receives BBClk from the RF circuitry 200.

The CDC 160 provides clock signals derived from BBClk to the BMC 120, the microcontroller 140 and the Serial Control Interface 110.

The Serial Control Interface 110 is controlled to produce DBus by either the microcontroller 140 or the Burst Mode Controller 120. The Burst Mode Controller controls DBus when time critical configurations to RF circuitry 200 are made. Whether the microcontroller 140 or the BMC 120 controls the content of DBus is determined by a switch signal 142 provided by the microcontroller 140 to the Serial Control Interface 110. The BMC 120 provides Data information 122, address information 124 and R/W information 126 to the Serial Control Interface 110 which places this information in the correct serial format on DBusDa. The clock signal DBusClk (13MHz) is received from Clock Distribution Circuitry. The timing of the transitions in the

Enable signal DBusEnX are controlled by a Trigger signal 132 provided by the Timing Control Unit 130 in the BMC 120.

The Burst Mode Controller 120 controls the content of RFBus1 and RFBus2 and may additionally control the content of DBus. It directly provides RFBus2 to pin 42 and provides RFBus1 to pin 40 in the Transmit Mode and receives RFBus1 from pin 40 in the Receive Mode.

The microcontroller may access the DBus and hence the RF circuitry via the Serial Control Interface. When the DBus is controlled by the microcontroller no time critical tasks can be controlled via the DBus. This configuration is used in the boot phase or for RSSI measurement. When the BMC 120 controls the DBus, it is possible to control time critical tasks via the DBus. The ability of the BMC 120 to control time critical tasks via the DBus depends upon the resolution of the trigger signal 132 which is at least 1μs. The control signals sent by the BMC 120 via RFBus2 may have an even higher resolution if they are directly clocked by BBClk @ 13MHz.

Interface of RF circuitry

Fig 1b illustrates the RF circuitry 200 which has an interface 10. The interface has pins 20, 22 and 24 dedicated respectively to DBusDa, DBusEnX and DBusClk, pin 30 dedicated to SleepX and pins 40, 42 and 44 respectively dedicated to RFBus1, RFBus2 and BBClk. The RF circuitry 200 includes a Control Interface 210; a register set 220 illustratively including registers 222, 224 and 226; decoding circuitry 230; a NOT gate 232; a two input AND gate 234; a three input OR gate 236; power-supply regulator circuitry 240; a reference oscillator 250; switching circuitry 260; Transmission Path 270 and Reception Path 280.

The Control Interface 210 has an input interface 212 connected to DBus and a input 214 for receiving Sleep X. It has an output 216 for supplying a mode control signal to the input of decoding circuitry 230 and to the control input 262 of the switching circuitry 260 and an interface 218 for accessing the set of registers 220. The Control Interface 210 receives DBus and performs the appropriate action which may involve writing to a register or reading from a register and changing the mode of operation of the RF circuitry 200. By writing to appropriate registers the Control Interface 210 may control the operational mode of the RF circuitry 200, control the synthesizer frequency in the Tx or Rx path, control whether the RF circuitry should receive or transmit, and control the power at which the Tx path 270 should transmit. By reading from appropriate registers information concerning received signal quality such as RSSI can sent by the Control Interface 210 to the BB circuitry 100. For simplicity of illustration the operative connections of the Rx Path 280 and Tx Path 210 to the register set 220 are not shown. A two bit signal is provided at the output 216 indicating the operational mode- [10] indicates Receive Mode, [01] indicates Transmit Mode and [11] indicates Control Mode.

The switching circuitry 260 has an input 262 connected to output 216 of the Control Interface 210, a single primary interface and three secondary interfaces. The primary interface has one port connected to pin 40 to transfer RFBus1 and another port connected to pin 42 to transfer RFBus2. One of the secondary interfaces is connected at any one time to the primary interface in dependence on the signal received at the input 262. When the signal at input 262 indicates Control Mode a port 264 of a first one of the secondary interfaces is connected to pin 40 via the switching circuitry 260. The port 264 is connected to one input of the AND gate 234. When the signal at input 262 indicates Transmit Mode a port 266 of a different one of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 267 of that secondary interface is connected to pin 42 via the switching

circuitry 260. When the signal at input 262 indicates Receive Mode a port 268 of another of the secondary interfaces is connected to pin 40 via the switching circuitry 260 and the other port 269 of that secondary interface is connected to pin 42 via the switching circuitry 260. The ports 266 and 267 and 268 and 269 are connected to the Tx Path 270 and Rx Path 280 respectively as further illustrated in Figure 1c.

The decoding circuitry 230 has a 2 bit wide input connected to the output 216 of the Control Interface 210 and provides its output to one input of AND gate 234 and, via NOT gate 232, to one input of OR gate 236. The decoding circuitry 230 produces a HIGH output when the signal received at its input identifies the Control Mode and a LOW signal otherwise.

The OR gate receives one input via the NOT gate 232 as described, another input from the pin 30 which receives SleepX and a final input from the output of AND gate 234. The output of the OR gate 236 is provided as a standby control signal to the Power-Supply Regulation Circuitry 240 and to the Reference Oscillator 250. A LOW output from the OR gate 236 places Power-Supply Regulation Circuitry 240 into a low power consumption standby state and switches the Reference Oscillator 250 off.

The Reference Oscillator 250 provides its output to the pin 44. It's output is also used elsewhere within the RF circuitry, but this is not illustrated for purposes of clarity.

Figure 1c illustrates the control effected on the Tx path 270 during Transmit Mode and the control effected on the Rx Path 280 during Receive Mode.

The Transmit path 270 includes Pulse Shaping Circuitry 272 which receives an input from port 266 of switching circuitry 260 in the Transmit Mode and

otherwise does not receive an input. The output of the Pulse Shaping Circuitry 272 is provided as an input to Modulation Circuitry 274 which provides the modulated signal to Power Amplifier 276 for amplification and subsequent transmission via an antenna. The power Amplifier 276 has a control input by which the amplifier gain may be forced to ramp up or ramp down. This control input is connected to port 267 of the switching circuitry 260. The power amplifier can therefore be switched on or off.

The Receive Path 280 includes Frequency Down Conversion Circuitry 286 which receives an input from the antenna in the Receive Mode. The circuitry 286 converts the received signal to a lower frequency and provides it to Demodulation Circuitry 284. The demodulated signal is provided to DC estimation circuitry 282. The amplitude decided data output by DC Estimation circuitry 282 is supplied to the port 268 of the switching circuitry 260. The DC Estimation Circuitry 282 has a control input connected to the port 269 of switching circuitry 260. The signals provided at the control input determine whether the DC Estimation operates in a fast mode or a slow mode.

Operational Modes

In the Transmit Mode, as illustrated in Figure 2b, RFBus1 and RFBus2 are driven by BB circuitry 100. RFBus1 supplies digital data for transmission <TXDATA> from BB circuitry 100 to RF circuitry 200 via pin 40. Logic levels are used and pulse shaping is done completely in RF circuitry 200. RFBus2 controls the timing of powering up the Power Amplifier (PA) in the RF circuitry 200 using control signal <PAON>. When RFBus2=<PAON>=HIGH the Power Amplifier is on when RFBus2=<PAON>=LOW the Power Amplifier is off. The switching on and off of the Power Amplifier is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 μs for Bluetooth Specification 1.0).

In Receive Mode, as illustrated in Figure 2c, RFBus1 is driven by RF circuitry 200 and RFBus2 driven by BB circuitry 100. RFBus1 supplies received data <RXDATA> to the BB circuitry 100 via pin 40. RFBus2 controls DC estimation in RF circuitry 200 via pin 42. The switching of DC estimation is 'time critical' as it occurs on a time scale of less than 1 slot duration. <DCTRACK>=LOW cause use of a fast acquisition of a DC estimate which is typically used at the start of a received packet and <DCTRACK>=HIGH controls use of a slower DC estimation which is typically used for the remainder of the packet. The change of DC estimation is 'time critical' as it must be controlled over time scales of less than 1 bit duration (1 μs for Bluetooth Specification 1.0).

The Control Mode is the neutral mode entered when neither the Transmit Mode or Receive Mode are active. It is entered when SleepX is LOW or via a control word on DBus. In this mode, as illustrated in Figure 2a, RFBus1 and RFBus2 are driven by BB circuitry 100: RFBus2 does not have an assigned functionality; RFBus1= <ClkOn>. When RFBus1=<ClkOn>=HIGH, AND gate 234 switches ON the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240. When RFBus1=<ClkOn>=LOW, AND gate 234 switches OFF the Reference Oscillator 250 and the Power Supply Regulation Circuitry 240 into standby. The RF circuitry is placed in a low power mode. There is no activity on DBus and RFBus and BBClk is switched off.

It will therefore be appreciated that the RFBus is used for different purposes during different operational modes of the system, as illustrated in Figures 2a, 2b, and 2c and Table 2.

The operation of a LPRF device is described in detail in UK Patent Application No 9820859.8 , the contents of which are hereby incorporated by reference. In particular Figure 4 shows LPRF RF components of a transceiver (Tx, Rx

and Frequency control), connected to baseband components (the remaining elements in the Figure).

In the preceding described embodiment, the receive path 280 was partitioned so that the DC Estimation circuitry 282 was in the RF Circuitry 200. This results in RFBus1, during the receive mode, transferring RxData from the RF Circuitry 200 to the BB circuitry 100 across interface 10 and RFBus2 transferring a control signal, DcTrack, from the BB circuitry 100 to RF Circuitry 200 across interface 10. This partitioning of the receive path is not essential.

In a second contemplated embodiment, the DC Estimation circuitry 282 is located within the baseband circuitry 100. This results in RFBus2 having a different directional flow than described above in the receive mode. In the second embodiment, the DCTrack signal is wholly within the baseband circuitry 100 and is not provided at the interface 10. The analog output of the demodulator 284 is converted to a digital signal for example by a sigma-delta converter whose outputs are mapped to RFBus1 and RFBus2. Consequently, in this embodiment, data flows on both RFBus1 and RFBus2 from the RF circuitry 200 to the baseband circuitry 100 via interface 10 during the receive mode.

It is further contemplated that RF circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

It is further contemplated that BB circuitry as described in the first embodiment may have additional circuitry which allows its functionality to be changed to operate in accordance with the second embodiment.

The present invention includes any novel feature or combination of features disclosed herein either explicitly or implicitly or any generalization thereof.

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made to the foregoing description without departing from the scope of the invention.

Claims

1. A device having an interface for controlling RF transceiver circuitry, the interface having:

a plurality of connectors for controlling the RF transceiver circuitry including providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;

at least first and second further connectors wherein in a first mode, one of said first and second connectors supplies data to the transceiver and the other is operable to perform a first function and wherein, in the second mode, one of said first and second connectors receives data from said RF module and the other is operable to perform a second different function.

2. A device as claimed in claim 1 wherein said first function is the provision of a first control signal to the transceiver

3. A device as claimed in claim 2 wherein the first control signal is a time critical control signal.

4. A device as claimed in any preceding claim wherein the first function is controlling the power amplifier of the transmitter portion of the transceiver.

5. A device as claimed in any preceding claim wherein said second function is the provision of a second control signal to the transceiver.

6. A device as claimed in claim 5 wherein the second control signal is a time critical control signal.

7. A device as claimed in any preceding claim wherein the second function is controlling dc estimation of the data received by the receiving portion of the transceiver.

8. A device as claimed in any one of claims 1 to 4 wherein said second function is the reception of data from the transceiver

9. A device as claimed in any preceding claim wherein the first connector is bi-directional and supplies data in the first mode and receives data in the second mode.

10. A device as claimed in any preceding claim wherein predetermined time critical control signals are not provided via said plurality of connectors.

11. A device as claimed in any preceding claim wherein the first mode is a transmit mode for the transceiver.

12. A device as claimed in any preceding claim wherein the second mode is a receive mode of the transceiver.

13. A device as claimed in any preceding claim wherein the plurality of connectors includes a connector for transferring data to and from the device, a connector for providing, an enable signal from the device and a connector for providing a clock signal from the device.

14. A device as claimed in any preceding claim wherein the plurality of connectors are used to read from and write to registers in the transceiver

15. A device as claimed in any preceding claim wherein the plurality of connectors is a serial interface having at least one connector via which data is transmitted serially, said data including a device address, a bit indicating whether data is for writing or is to be read, a local address and a variable data portion.

16. A device as claimed in any preceding claim, further comprising first control circuitry and a processor, wherein the first control circuitry is arranged to control the RF circuitry via the plurality of connectors and/or the first and second further connectors and the processor is arranged to control the RF circuitry only via the plurality of connectors.

17. A device as claimed in claim 15 wherein the data portion may have a length varying between 1 and 32 bits.

18. A device as claimed in any preceding claim wherein the plurality of connectors are coupled to at least one other device.

19. A device as claimed in any preceding claim further comprising a connector for receiving a clock signal from the transceiver.

20. A device as claimed in any preceding claim having a third connector (SleepX) for powering down components of the transceiver.

21. Transceiver circuitry having an interface for connection to a device having baseband circuitry, the interface having:

a plurality of connectors for providing control information for changing the mode of operation of the transceiver, said modes including a transmit mode and a receive mode;

at least first and second connectors wherein in a first mode, data is received at one of said first and second connectors and the other performs a first function and wherein, in the second mode, data is provided at one of said first and second connectors for transfer to the device and the other performs a second function different to the first.

22. Transceiver circuitry as claimed in claim 21 having a power amplifier, wherein the first function is the reception of a first control signal for controlling the power amplifier.

23. Transceiver circuitry as claimed in claim 21 or 22 having DC estimation circuitry wherein the second function is the reception of a second different control signal for controlling the dc estimation circuitry.

24. Transceiver circuitry as claimed in claim 21 or 22 wherein the second function is the provision of received data.

25. A method of interfacing a device having baseband circuitry to transceiver circuitry, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the transmitting mode;
providing data from the device to the transceiver via the first connector; and
controlling the power amplifier in the transceiver via the second connector.

26. A method of interfacing a device having a baseband engine to a transceiver, the device having means for controlling whether the transceiver is in a transmitting mode or a receiving mode and first and second connectors, comprising the steps of:
controlling the transceiver to enter the receiving mode;

receiving data at the device from the transceiver via the first connector; and controlling the dc estimation in the transceiver via the second connector.

27. An interface having connectors including a first connector arranged to transfer a signal for controlling time critical functions and a second connector arranged to transfer data, said time critical function being dependent upon whether the second connector is receiving or providing data.

TABLE 1:
SUMMARY OF THE INTERFACE SIGNALS

PIN	NAME	DIRECTION	FUNCTION
20	DBusDa	BIDIRECTIONAL	CONTROL INTERFACE: DATA
24	DBusClk	BB -> RF	CONTROL INTERFACE: CLOCK
22	DBusEnX	BB -> RF	CONTROL INTERFACE: ENABLE
40	RFBus1	BIDIRECTIONAL	DATA INTERFACE: LINE 1
42	RFBus2	BB -> RF	DATA INTERFACE: LINE 2
44	BBCLK	RF -> BB	DATA INTERFACE: CLOCK (e.g. 13 MHz)
30	SleepX	BB -> RF	SLEEP-MODE CONTROL & REST

TABLE 2:
OPERATING MODES AND THEIR INFLUENCE ON THE DATA INTERFACE

MODE NAME	FUNCTIONALITY OF RFBUS1	FUNCTIONALITY OF RFBUS2	DIRECTION OF RFBUS1	DIRECTION OF RFBUS2
CONTROL MODE	<CLKON>	0	BB → RF	BB → RF
TRANSMIT MODE	<TXDATA>	<PAON>	BB → RF	BB → RF
RECEIVE MODE	<RXDATA>	<DCTRACK>	BB ← RF	BB → RF

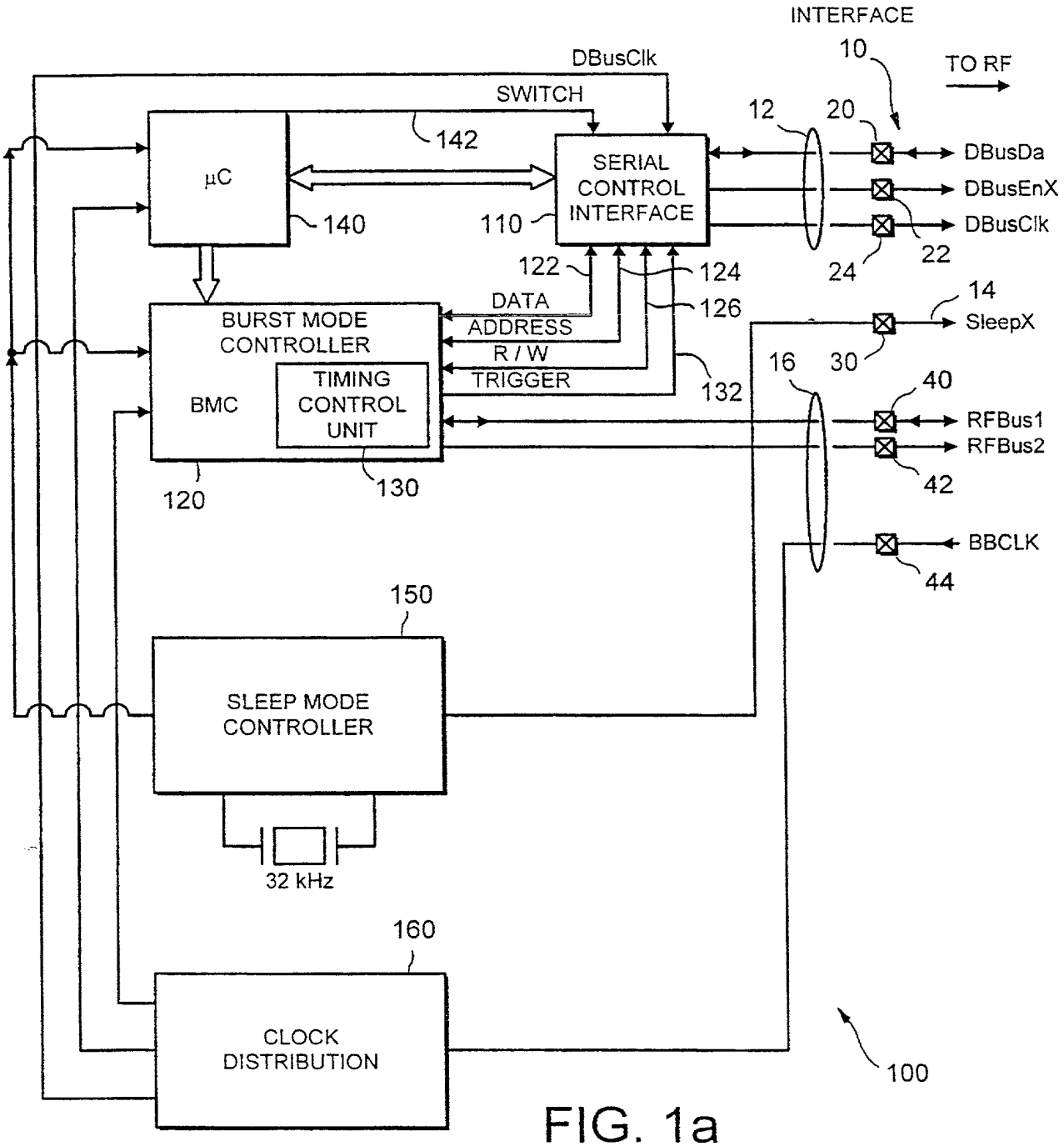
INTERFACE
10
TO RF
DBusClk
SWITCH
142
12
20
μC
140
SERIAL CONTROL INTERFACE
110
DBusDa
DBusEnX
DBusClk
22
24
122
124
126
DATA
ADDRESS
R / W
TRIGGER
132
14
SleepX
30
BURST MODE CONTROLLER
BMC
TIMING CONTROL UNIT
16
40
RFBus1
RFBus2
42
120
130
BBCLK
44
150
SLEEP MODE CONTROLLER
32 kHz
160
CLOCK DISTRIBUTION
100

FIG. 1a

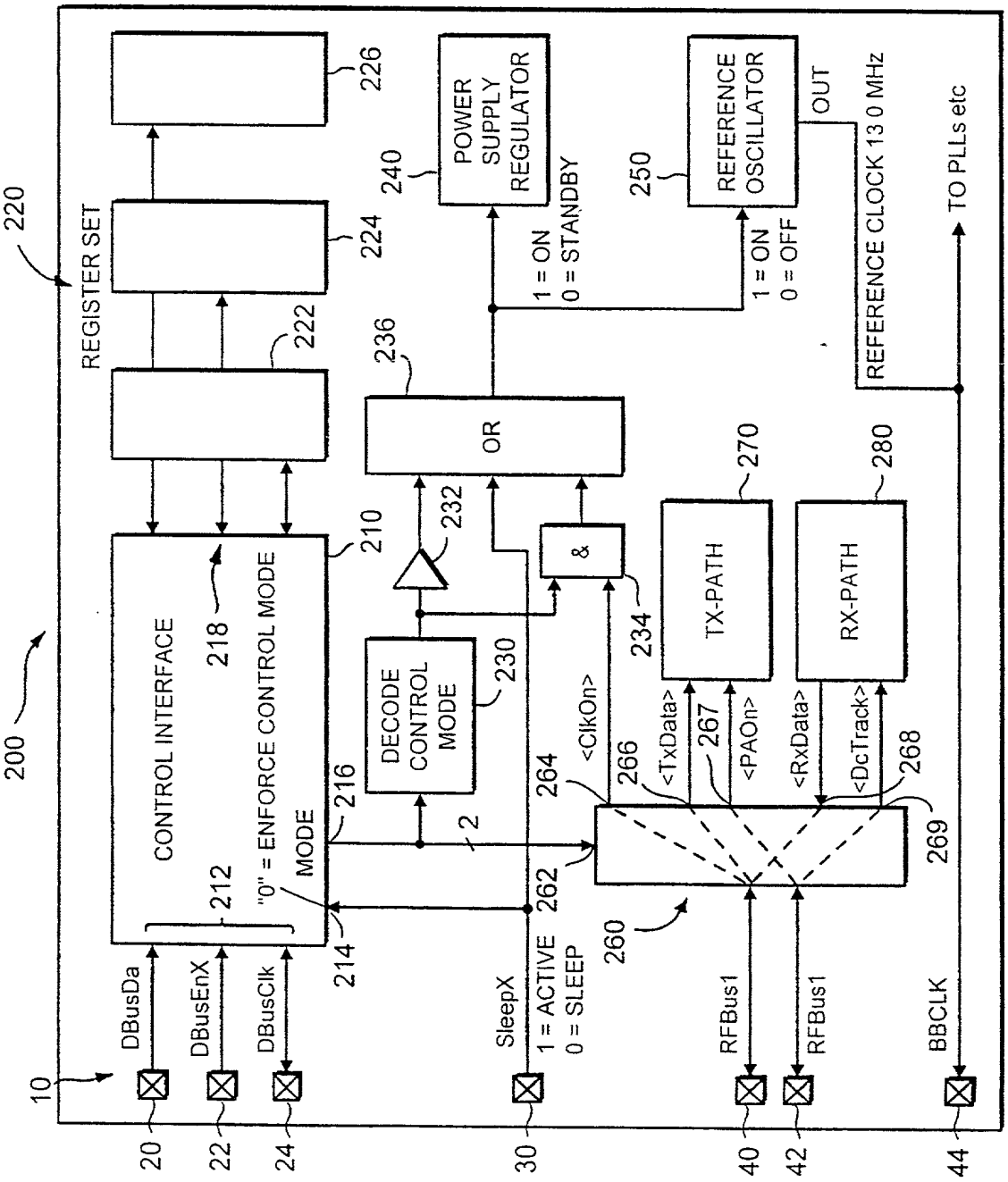
200
10
220
REGISTER SET
226
224
222
CONTROL INTERFACE
218
"0" = ENFORCE CONTROL MODE
MODE
212
214
210
216
DECODE CONTROL MODE
230
232
OR
236
&
234
POWER SUPPLY REGULATOR
240
1 = ON
0 = STANDBY
REFERENCE OSCILLATOR
250
OUT
1 = ON
0 = OFF
REFERENCE CLOCK 13 0 MHz
TO PLLs etc
TX-PATH
270
RX-PATH
280
<ClkOn>
264
<TxData>
266
<PAOn>
267
<RxData>
<DcTrack>
268
269
260
262
2
DBusDa
DBusEnX
DBusClk
SleepX
1 = ACTIVE
0 = SLEEP
RFBus1
RFBus1
BBCLK
20
22
24
30
40
42
44

FIG. 1b

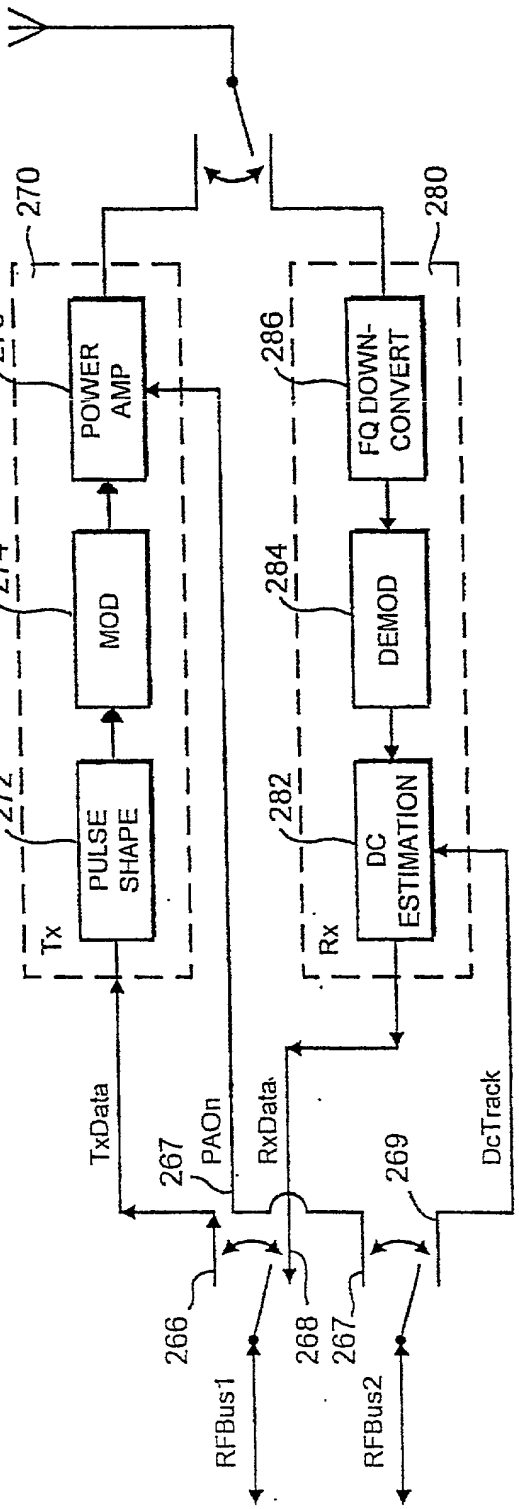

FIG. 1c

IN Tx Mode - SWITCHES UP

IN Rx Mode - SWITCHES DOWN

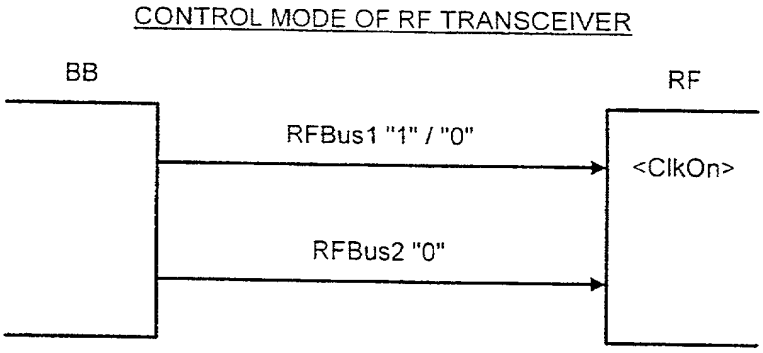

FIG. 2a

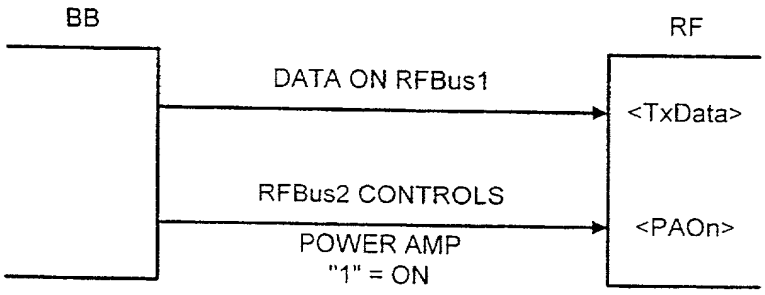

FIG. 2b

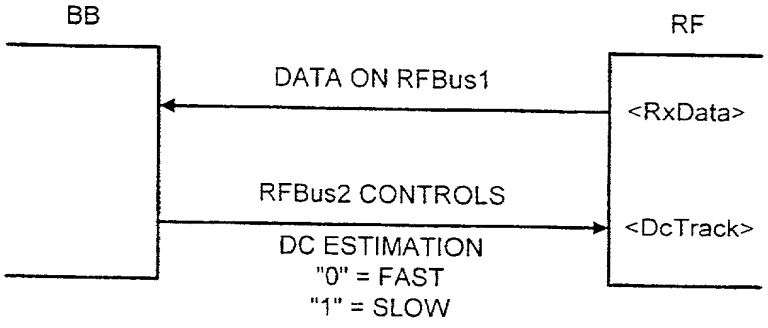

FIG. 2c

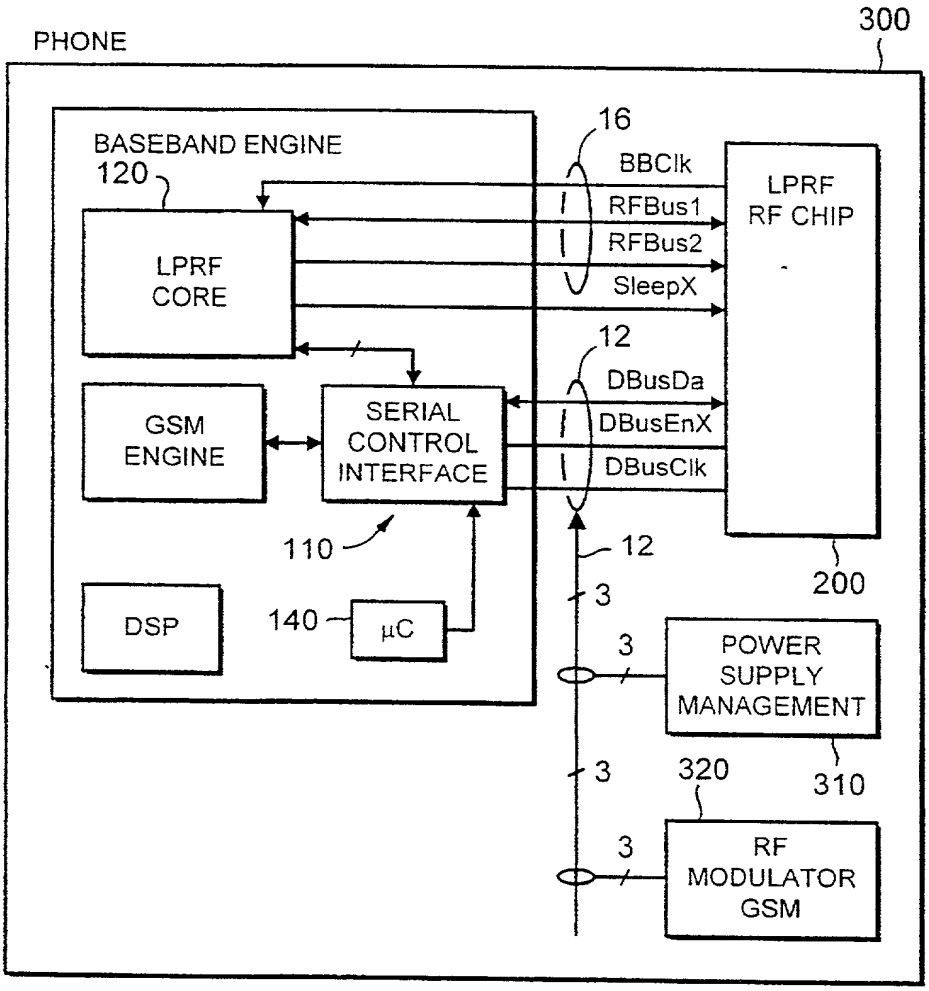
PHONE
300
BASEBAND ENGINE
120
LPRF
CORE
GSM
ENGINE
SERIAL
CONTROL
INTERFACE
110
DSP
140
µC
16
BBClk
RFBus1
RFBus2
SleepX
12
DBusDa
DBusEnX
DBusClk
LPRF
RF CHIP
200
12
3
3
POWER
SUPPLY
MANAGEMENT
310
3
320
3
RF
MODULATOR
GSM

FIG. 3

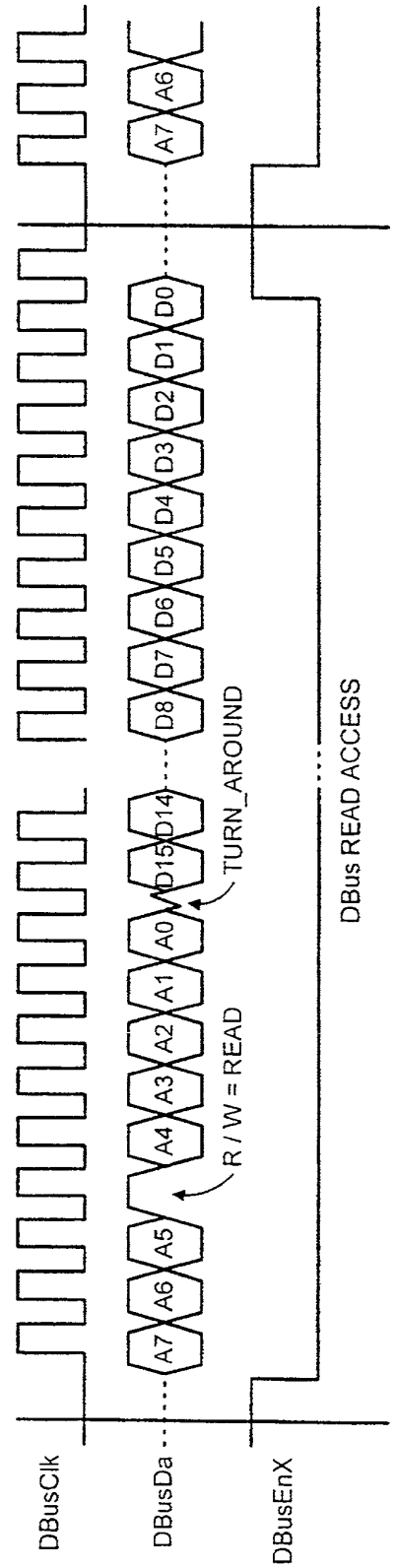
DBusClk
DBusDa
DBusEnX
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D8
D7
D6
D5
D4
D3
D2
D1
D0
R / W = READ
TURN_AROUND
DBus READ ACCESS

FIG. 4a

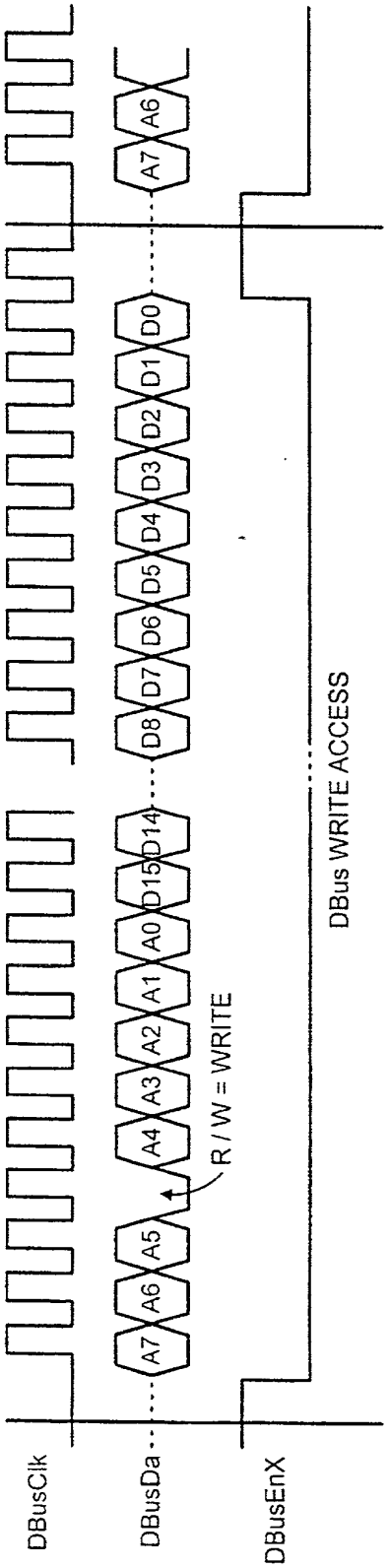
DBusClk
DBusDa
DBusEnX
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D8
D7
D6
D5
D4
D3
D2
D1
D0
R / W = WRITE
DBus WRITE ACCESS

FIG. 4b

Please type a plus sign (+) inside this box → [+]

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Filing Date	July 13, 2001
First Named Inventor	LINDLAR, et al
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Signature	Donald E. Stout	
Date	July 13, 2001	

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DECLARATION AND POWER OF ATTORNEY - PATENT APPLICATION

As a below named inventor, I hereby declare: that my citizenship, residence and post office address are as stated below; that I verily believe I am the original, first and sole inventor (if only one is named below) or a joint inventor (if plural inventors are named below) of the invention entitled: Inteface

the specification of which ___ is attached hereto

___ was filed on 13 July 2001 as Application Serial No. 09/889,232 and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a). I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
9900829.4	GB	15/01/1999	Yes
9928574.4	GB	03/12/1999	Yes
9928856.5	GB	07/12/1999	Yes
Number	Country	Day/Month/Year Filed	Yes / No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application;

Application Serial No	Status-patented, pending or abandoned

I hereby appoint as principal attorneys: Donald R. Antonelli, Reg. No. 20,296; David T. Terry, Reg. No. 20,178; Melvin Kraus, Reg. No. 22,466; William I. Solomon, Reg. No. 28,565; Gregory E. Montone, Reg. No. 28,141; Ronald J. Shore, Reg. No. 28,577; Donald E. Stout, Reg. No. 26,422; Alan E. Schiavelli, Reg. No. 32,087; James N. Dresser, Reg. No. 22,973, Carl I. Brundidge, Reg. No. 29,621; and Paul J. Skwierawski, Reg. No. 32,173; to prosecute and transact all business in the Patent and Trademark Office connected with this application and any related United States and international applications.

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Suite 1800
1300 North Seventeenth Street
Arlington, Virginia 22209

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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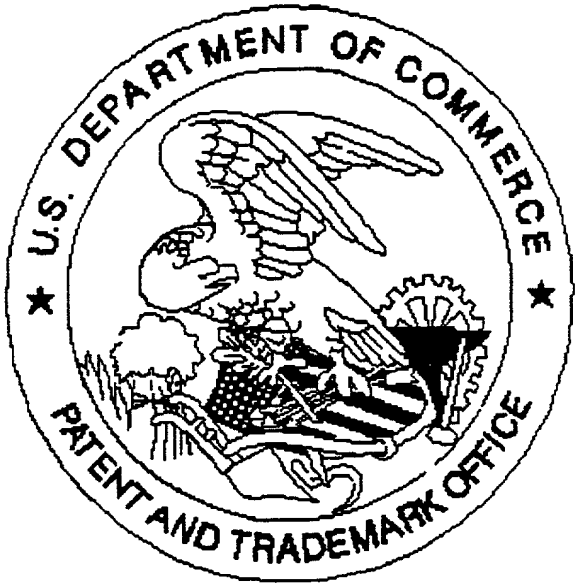

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